CMPE 124 Lab 6: Counter Design with D and JK Flip-Flops

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***Abstract* —** The purpose of this lab is to design a circuit with D and JK Flip-Flops to get more practice with those two parts.

# INTRODUCTION

For this lab’s requirement, it is designing about D and JK flipflop two divide-by-two circuits, one-clock-period-delay with D flipflop, and three-bit ripple down counter.

# Design methodology

For the divide-by-two circuit, we know that both D and JK Flipflop can store value for one clock period when the clock is in rising edge triggered. In order to build this circuit, the output of D flip flop is feeding back to the input. D flip flop with one clock period delay is also followed the same strategy. Besides, the output of the flipflop is connected to the input of other flipflop.

## Parts List

* SN74HC74
* SN74HC109
* SN74HC163AN
* Crystal FS10.00P
* 1KΩ Resistors
* 100pF capacitor

## True table

Not applicable

## Kmap

Not applicable

## Original and Derived Equations

Not applicable

## Schematics



**Figure 1**: Two-divide-two circuit using D Flip-Flop



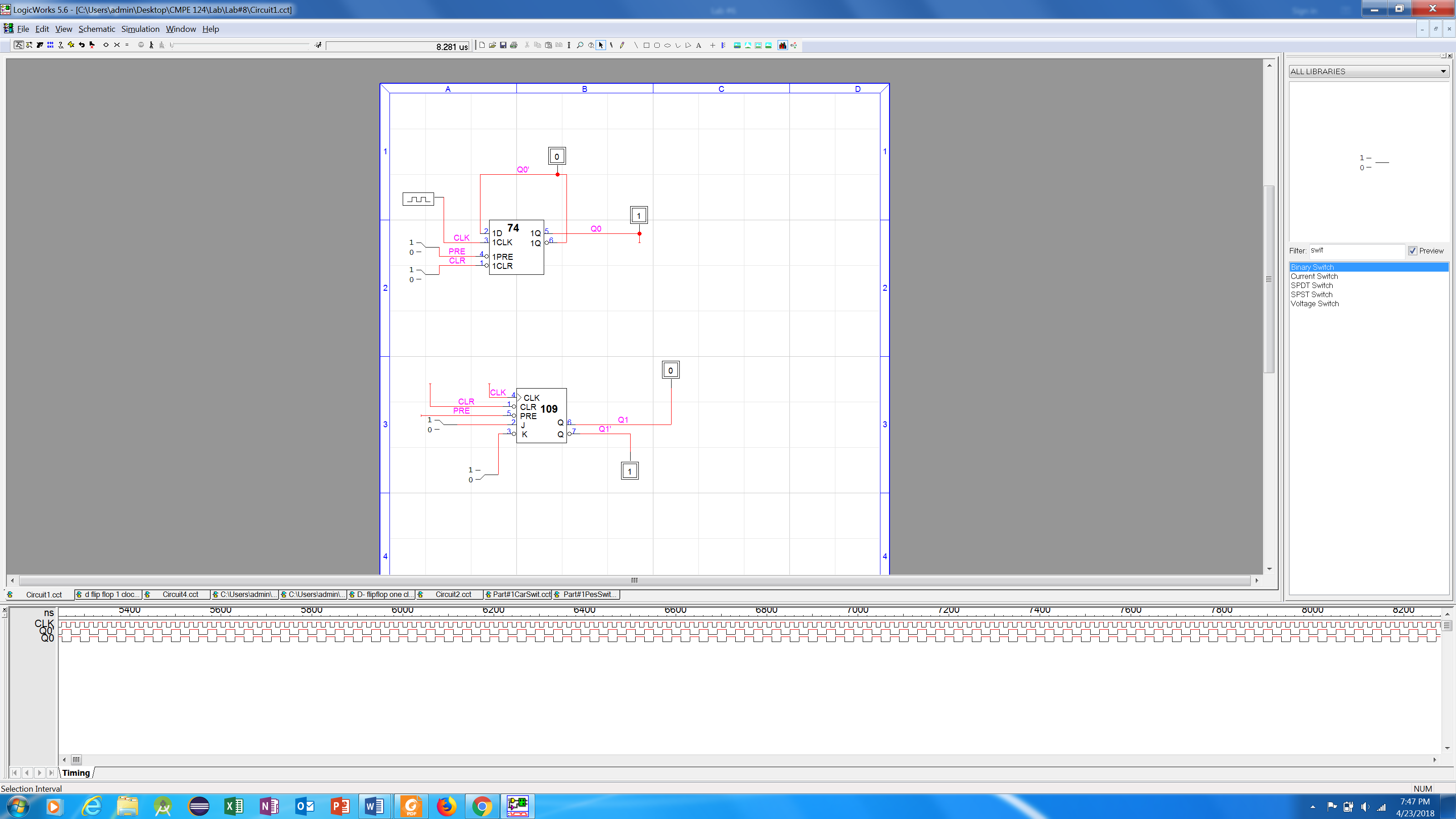
**Figure 2**: Two-divide-two circuit using JK Flip-Flop

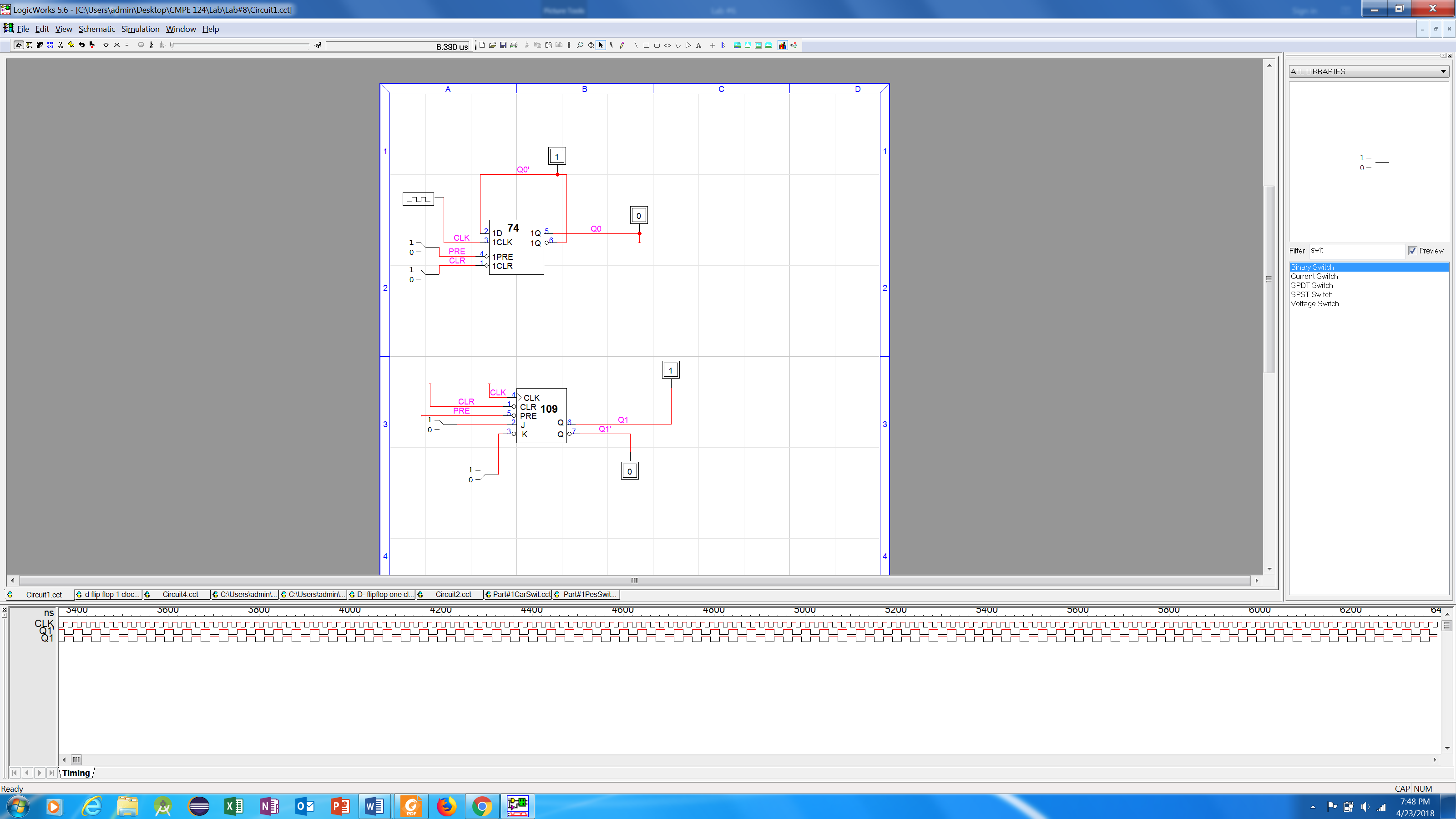
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**Figure 3:** Design one-clock-period-delay circuit using D Flip-Flop

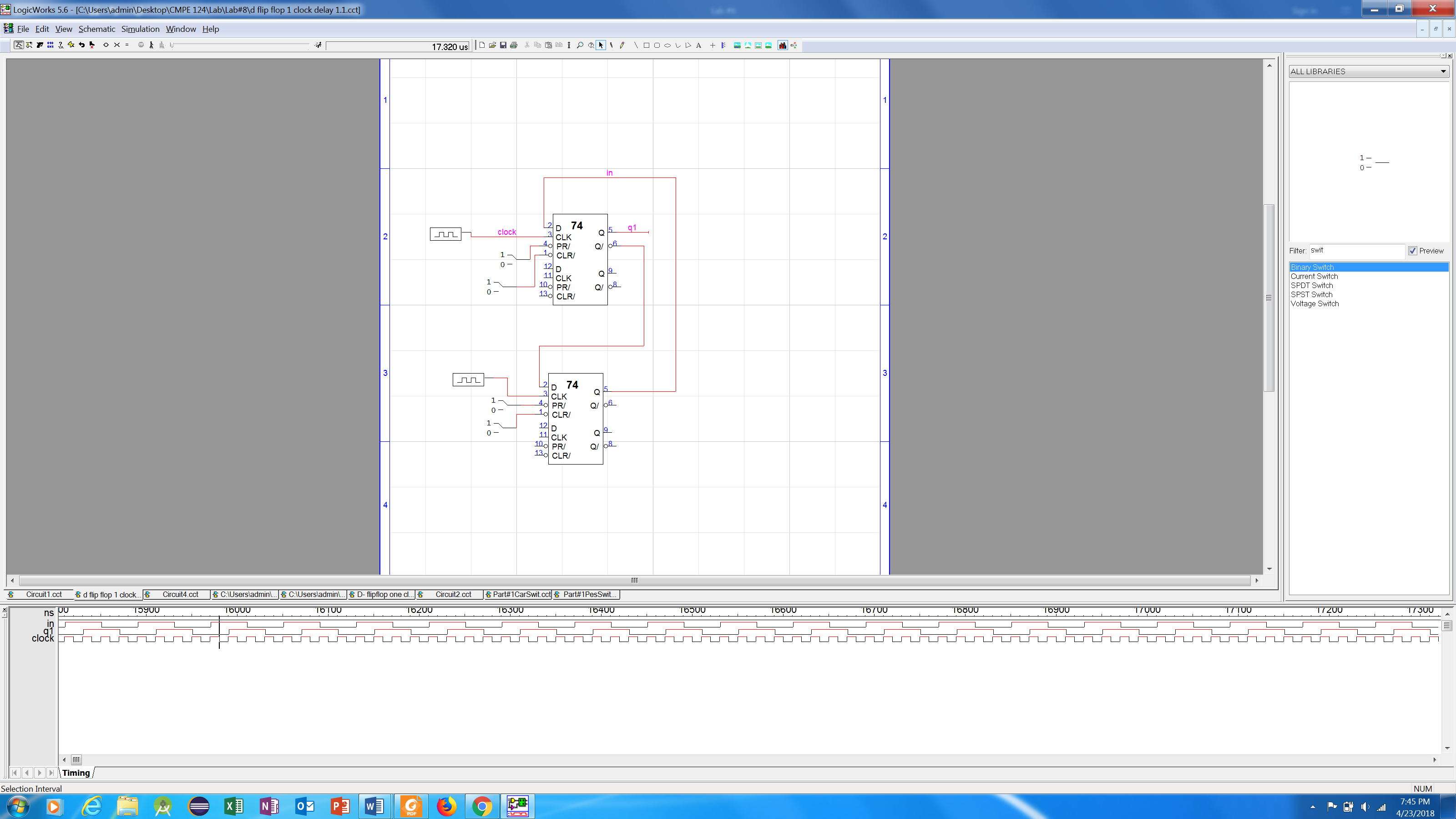
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**Figure 4:** Three bits JK flip-flop ripple down counter using JK Flip-Flop

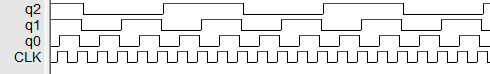
**Figure 5**: Divide-by-two circuit with D flip-flop



**Figure 6** : Divide-by-two circuit with JK flip-flop



**Figure 7**: One clock period with D flip-flop



**Figure 8**: Three bit ripple down counter with JK flipflop

# testing procedure

Step1: Build the circuit two-divide-two with D and JK flip-flip on Logic Work and observing the output waveforms from Q and clock. After that, comparing the waveform of Q and clock.

Step 2: Build the one-clock-period-delay circuit using D Flip-Flop on logic work and also observer the output of Q and clock

Step 3: Watching the waveform of JK flip flop with three-bit ripple down counter. Compare the waveform of the clock with each output

# testing results

1. The result of testing of the two-divide-two by using D flipflop and JK flip flop are showed in the figure 5 and 6.
2. The result of D flip-flop’s one clock period is showed in figure 7.
3. The result of JK flip-flop’s one clock period is showed in figure 8.

# Conclusion

Throughout the lab, student have learned how to build two-divide-two circuit, one clock delay and three bits counter down circuit. The lab is finished successful and in expectation. After finishing this lab, student could achieve and understand more about logic work.

1. appendices and References